Amplifier Function Block

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Understanding and Using the CALEX Instrumentation Amplifier Function Block

Abstract

The instrumentation amplifier block is common to many CALEX function modules including the model 176 instrument amplifier. This note provides a detailed theory on how the amplifiers work and additional application information.

Instrumentation Amplifier Operation

The CALEX instrumentation amplifier block is built around the classical current feedback differential amplifier. These amplifiers serve the needs of high precision analog voltage amplification while maintaining very high input impedance.

This circuit consists of (Figure 1) two matched monolithic input transistors Q1 and Q2, a differential to single ended converter A1 and a common mode feedback amplifier A2. Figure 2 shows a simplified schematic diagram of the amplifier with current feedback. In Figure 2 the input signal to be amplified is impressed across the differential inputs +INPUT and -INPUT. This voltage is essentially transferred to the gain setting resistor R_G by the emitter follower action of the input pair.

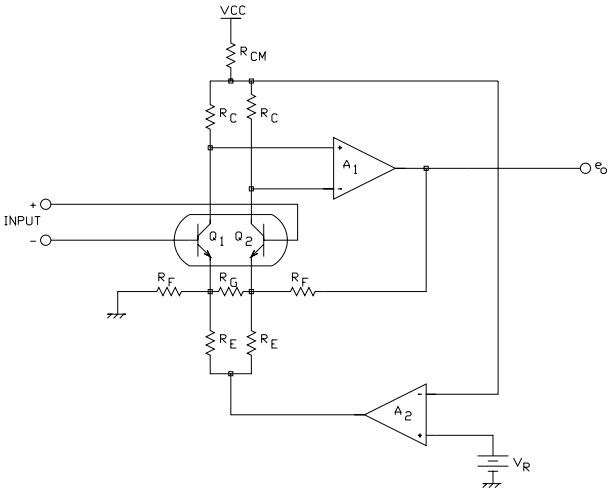


FIGURE 1. Simplified Instrumentation Amplifier

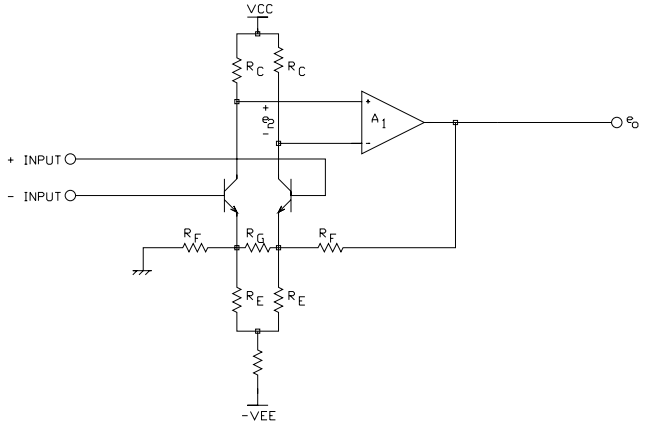


FIGURE 2. Current Feedback Block

Initially this transfer creates an imbalance in the input pair base emitter voltages and a like imbalance in the collector currents. The error current creates a voltage difference at the input terminals of amplifier A1. This amplifier differential to single ended conversion function and its feedback is such that it will move the output terminal in a direction so that an equal offsetting current to the original imbalance will be developed through R_F . This current feedback action then always works to keep the input pair base emitter voltages the same by sending the difference between the collector resistors voltage drop and applying feedback to make the differential drop (e2) equal to zero. At this point the gain of the amplifier can be written as,

$$Av = 1 + \frac{2 \times R_F}{R_G} + \frac{R_F}{R_E}$$

R_F/R_E is chosen to be equal to 9 +0.05% and since R_F is 100,000 ohms the gain equation is reduced to,

$$Av = 10 + \frac{200K}{R_G}$$

While this simplified block diagram seems to work well it can have significant common mode and linearity errors.

The linearity errors are mostly due to input transistor mismatching, and these errors are held to 50 ppm (Parts Per Million) or 0.005% by the use of a dual monolithic 'Supermatched Pair' in the CALEX amplifiers.

The common mode errors are due to mismatching in the collector and feedback resistors (R_C and R_F) and in the input pair. To achieve common mode rejections greater than 100 dB at frequencies from DC to 60 Hz would have required unrealistic matching in the resistor ratios and transistor parameters. An active common mode correction technique was developed to sense the common mode voltage and drive the bottom of the input pair so that the whole input stage is constantly impressed with the same voltage (V_R).

This reduced the required matching of the resistors and transistors with respect to voltage operating point changes and helps to cancel out parasitic capacitance effects that would otherwise degrade common mode performance with frequency. The only two critical resistors are then the feedback resistors since they are both still impressed with the full common mode voltage swing.

Amplifier DC Considerations

An instrumentation amplifier is used where high input impedance is required, where large common mode signals may be present and must be rejected and where low level signals are to be amplified with very high accurate gains with a minimum of distortion (low nonlinearity).

To this end a few guidelines are in order to optimize DC performance of instrumentation amplifiers.

1) Use shielding techniques for high (> 1k ohm) impedance transducers.
2) Connect the low side of a bridge transducer to the structure which it is mounted to. This prevents unwanted pickup from capacitative coupling to the bridge.
3) Use a 'Balanced Impedance' arrangement whenever possible. This balances out noise signals and will not degrade the amplifier common mode rejection ratio. The CMRR of an instrumentation amplifier is reduced with an unbalanced impedance on the input terminals. Keep the unbalance under 500 ohms. If the noise still persists add a small capacitator directly across the amplifiers input terminals.
4) A path must be provided for the input bias currents. Make sure that there is a current path from the inputs to signal common. Be careful to supply this path without degrading the amplifiers normal or common mode impedance to the point where errors arise.
5) Minimize the errors due to output circuit currents, and power supply ground returns by keeping these connections short and keeping a check on where the ground currents are flowing. Using single point grounds helps a great deal with these problems.

Amplifier Bandwidth Considerations

Since some gain is provided by the input pair the single ended converter can operate at lower closed loop gains thus extending the overall gain bandwidth product (GBP) to about 1 MHz. The -3 dB bandwidth for any other gain can be calculated by use of the following formula,

$$bw = \frac{GBP}{Gain}$$

bw = Resulting bandwidth
Gain = User desired gain

The overall response of the amplifier approximates that of a single pole rolloff. In some high accuracy applications AC signals must be amplified with very high precision. The real effective signal bandwidth then might be less than the -3 dB bandwidth because at the -3 dB point the gain is reduced by 30% and the phase shift is about -45 degrees. Figure 3 shows the gain error as a function of the signal frequency to -3 dB bandwidth ratio.

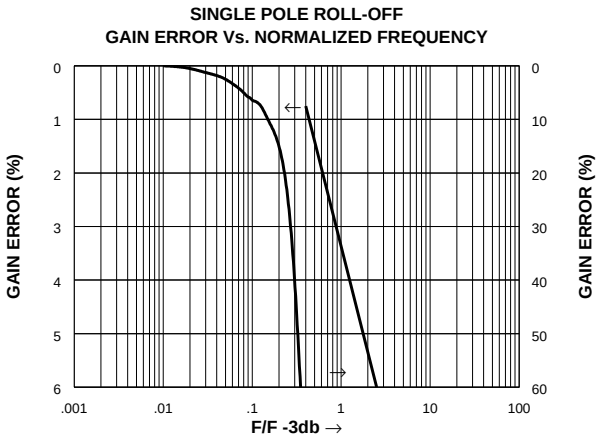


FIGURE 3. Gain Error as a Function of Frequency

For example: In a bicycle efficiency experiment [1] a strain gage was applied to the seat post of a test bicycle in an effort to determine relative efficiencies of various drive train components and designs. The range of frequencies that are expected are twice the pedaling rate or cadence of the test rider. These cadence rates can be as high as 110 RPM in this test.

If the signals are required to be accurate to 0.1 %, at how high a gain can the strain gage amplifier be run?

Since the data rate is twice the cadence the data rate is 3.7 cycles per second maximum (220/60 = 3.7). To capture all of the possible harmonics of the mechanical system the data rate is multiplied by a factor of 10 to yield a maximum data rate of 37 Hz. The maximum bandwidth ratio can be read off of Figure 3 as 0.045 of the system gain bandwidth product. Since the system gain bandwidth product is 1 MHz the maximum gain can be calculated as,

bw required = bw signal / 0.045
= 37 / 0.045
= 822 Hz

A_v Maximum = GBP / bw required
= 1 MHz/822
= 1200 Volts/Volt

The maximum gain that can be used and still not distort the signal beyond 0.1% is 1200 Volts/Volt. This would be plenty of gain for this application and in fact the amplifier is only capable of producing a gain 1000 maximum, but the advantage of a wide bandwidth instrumentation amplifier can be seen from this example.

What if the signals to be recorded are slow such as the output of a strain gage industrial scale such as might be used in a food processing plant.

What is the required system bandwidth if the system designer wants the weight reading to be stable to within 0.1% in 0.5 seconds after the scale is loaded but also does not want any more display jitter than necessary?

As shown in Figure 6, settling time to 0.1% will take 6.9 time constants (assuming this is a one pole response system) so the time constant of the amplifier is required to be:

Tc = T setting / 6.9
= 0.5 / 6.9
= 0.072 Seconds

The bandwidth is related to the system time constant by the following formula,

$$bw = \frac{0.159}{Tc}$$

so for our system the required bandwidth is,

$$bw = \frac{0.159}{0.072} = 2.2Hz$$

This is pretty low and it is clear that the instrument amplifier will easily amplify this signal at any gain, but it will also amplify a lot of unwanted signals too, causing the scale value to constantly 'jitter'.

What is needed is a way of bandlimiting these unwanted signals so that the desired information is not lost in the noise. With the CALEX line of instrumentation products bandlimiting can be accomplished in two ways: the easy way and the better way.

The easy way requires the least amount of money and extra components but has drawbacks in terms of overall system performance. The better way involves the addition of an active filter stage to the output of the amplifier. This provides the most repeatable control on bandwidth and does not degrade any other performance parameter.

Starting with the easy way first, referring back to Figure 1 it can be seen that the amount of gain is proportional to the value of RF if a capacitor is added across RF than the gain would drop with increasing frequency until it reaches a low value of 1.

The -3 dB bandwidth of the gain stage will be the frequency when the impedance of the capacitor exactly equals the value Of RF Hence the following equation can be written,

$$\frac{1}{2 \times \pi \times F \times C} = R_F$$

and solving for F the bandwith,

$$F = \frac{1}{2 \times \pi \times R \times C}$$

the system bandwith can be made to drop to 1 with a single pole response by the addition of a single capacitor across R_F but, this has the unfortunate side affect of decreasing the common mode rejection of the stage with increasing frequency. This is because the R_F on the other side of the input pair is now not equal to the shunted R_F.

The amount that the common mode performance is decreased is proportional to,

$$\frac{R_F \times Ad}{\Delta R_F}$$

where Ad is the gain (Ad = 10 + 200K/R_G) and ΔR_F is the mismatch in the values of RF on each side of the input pair. This mismatch remains unchanged for DC common mode signals but as the frequency of the common mode signals increases the mismatch gets larger because the capacitor across R_F is decreasing the impedance effectively making R_F smaller.

If the R_F on the other side of the pair can also be shunted by a capacitor of like value, both sides will drop in impedance with frequency and if the matching is perfect then the CMRR should remain unchanged at the original value. In practice the two sides will not match exactly because of the capacitance mismatch of the shunt capacitors.

Two ways to deal with this problem are 1) use high stability high accuracy matched capacitors or 2) use high stability 5 or 10 % capacitors and actively trim out the CMRR to a high value at 60 Hz or 120 Hz since this is where most unwanted common mode signals are. The trim can be accomplished by a trimmer capacitor or by using small capacitors in parallel with the larger shunt capacitor.

In the present example, to get a 2.2 Hz response a 0.7 micro Farad capacitor would be needed. The nearest standard value is a 0.68 micro Farad value. With this large a capacitor the second trim method is needed and if the capacitors have an initial accuracy of 5% then up to 5% of that value may be needed as trim (0.034 µF). The resulting circuit is shown in Figure 4.

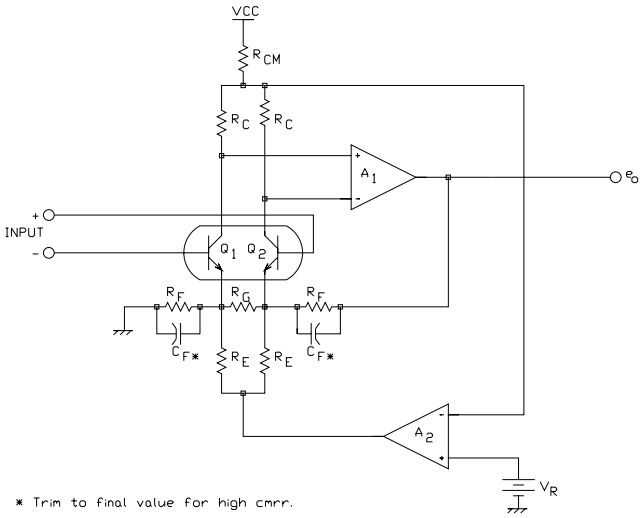
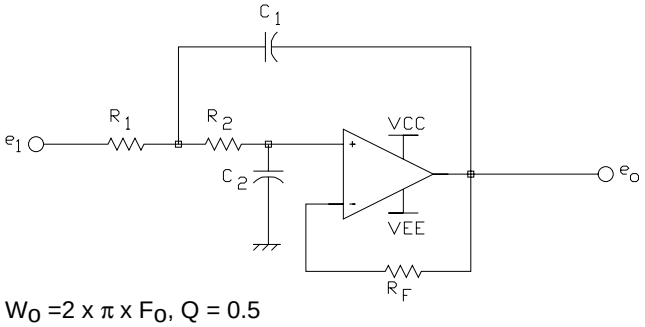


FIGURE 4. Bandlimiting the Gain Block

The simple way of bandlimiting provides a low cost way of bandlimiting the signals with the following limitations, 1) the gain will fall with increasing frequency to unity and 2) the CMRR must be trimmed after assembly if high CMRR is needed.

The better way of bandlimiting is to add an active filter stage to the output of the amplifier stage. Such an active filter is shown in Figure 5.



$W_O = 2 \times \pi \times F_O$, Q = 0.5

$C_1 = C_2 = C$ A Convenient Value

Then,

$$R_2 = \frac{1}{W_O \times C}$$

And,

$$R_1 = \frac{1}{W_O^2 \times C^2 \times R_2}$$

$R_F = R_1 + R_2$

FIGURE 5. 2nd Order Active Filter

This filter exhibits much improved roll-off of unwanted signals by adding two poles to the system and gain with increasing frequency will continue to fall below unity. This method of bandlimiting also does not affect the instrumentation amplifier common mode rejection ratio, but in fact attenuates the common mode signals with the same vigor as the unwanted normal mode signals thereby actually increasing the effective CMRR of the system.

Since two poles are used with this stage instead of one, our bandwidth equation must be modified by multiplying the desired bandwidth by 1.414, to achieve the same settling time.

As a sample design using the previous example the modified bandwidth is now,

bw design = 1.414 x bw calculated
= 1.414 x 2.2
= 3.11 Hz

solving for the equations in figure 5.

R1 = 51,000 C1 = 1.0 µF
R2 = 51,000 C2 = 1.0 µF
Rf = 100,000

any type of low noise op-amp may be used.

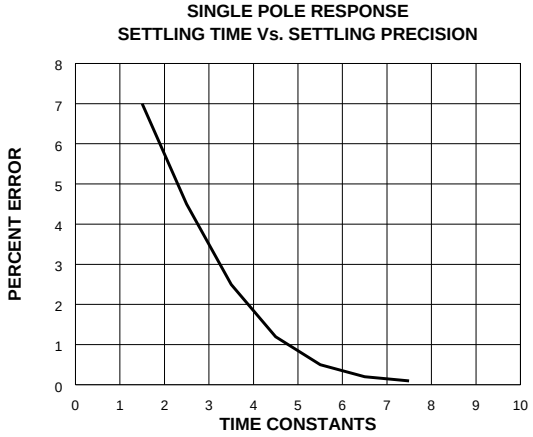
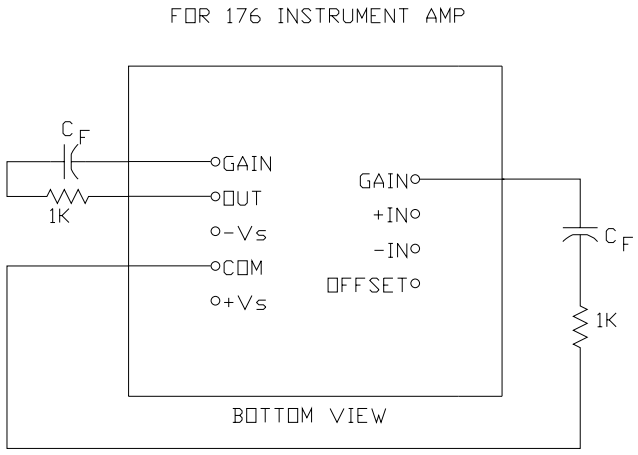


FIGURE 6. Settling Time Vs. Precision

Appendix A

Simple bandwidth limit shunt capacitor locations



References

[1] Biomechanics of shifting performance, Shinpei Okajima, BIKE TECH, April 1985; Rodale Press, Emmaus, Pa.